In the Specification:

Please replace the paragraph at page 10, lines 7-23 with the following amended paragraph:

The ferroelectric pattern 79 may be PZT(Pb, Zr, TiO_3) that si formed using $PbTiO_3$ as a seed layer. The ferroelectric pattern 79 may alternatively be formed from at least one material selected from the group consisting of Pb(Zr, Ti)O_3, $SrTiO_3$, $BaTiO_3$, (Ba, Sr)TiO_3, Pb(Zr,Ti)O_3, $SrBi_2Ta_2O_9$, (Pb,La)(Zr,Ti)O_3, and $Bi_4Ti_3O_{12}$. A PZT and $PbTiO_3$ thin layer may be formed using CSD. The CSD process may use as a precursor lead acetate[$Pb(CH3CO_2)_2$ $3H_2O$], zirconium n-butoxide [$Zr(n\text{-}OC_4H_9)_4$], and titanium isopropoxide [$Ti(i\text{-}OC_3H_7)_4$], and ~~as~~ using a solvent 2-methoxyethano [$CH_3OCH_2CH_2OH$]. Thin PZT and $PbTiO_3$ layers may be stacked using, for example, spin coating and baking at about 200°C. The resultant structures may be annealed using, for example, rapid thermal processing (RTP) in an oxygen atmosphere of 500 to 675°C. The resulting ferroelectric pattern 79 may exhibit an improved ferroelectric characteristics, and which may allow a corresponding reduction in the thickness of the ferroelectric pattern 79 and, thereby, a reduction in the thickness of the ferroelectric capacitor. Reducing the thickness of the ferroelectric capacitor 82 allows the sidewalls of the ferroelectric capacitor 82 to be patterned to be substantially vertical sidewalls or close to vertical. For example, the ferroelectric pattern 79 and the ferroelectric capacitor 82 may have respective thicknesses of 100nm or less and 400nm or less.